ABSTRACT OF THE DISCLOSURE

An electronic tester with digital, and analog, and memory test circuitry on a single platform. A test head is coupled to a device under test. The device under test can be a system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, or an analog integrated circuit. Digital test circuitry applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals. Analog test circuitry applies analog test signals to the device under test coupled to the test head and receives analog outputs from the device under test in response to the analog test signals. Memory test circuitry applies memory test patterns to the device under test coupled to the test head and receives memory outputs from the device under test in response to the memory test patterns. A tester computer supervises the application of digital, analog, and memory test signals from the digital, analog, and memory test circuitry to the device under test such that signals applied to the device under test can be solely digital test signals, solely analog test signals, solely memory test signals, or mixed digital, analog, and memory test signals. The test head, the digital test circuitry, the analog test circuitry, the memory test circuitry, and the computer are operable as a single platform.